

# AN OPTIMAL FPGA IMPLEMENTATION OF BSS NEURAL NETWORK MODEL. ICA – BASED APPROACH.

*Mouloud Ounas<sup>1</sup>, Salim Chitroub<sup>2</sup> and Rachida Touhami<sup>1</sup>*

<sup>1</sup>Instrumentation Laboratory, <sup>2</sup>Signal and Image Processing Laboratory  
Electronics and Computer Science Faculty, U. S. T. H. B.  
P. O. Box 32, El - Alia, Bab - Ezzouar, 16009, Algiers, Algeria

# PROBLEM STATEMENT

- The advanced technology of Very Large Scale Integration (VLSI) circuit design pointed an important effect in the development of complex digital circuit for Digital Signal Processing (DSP) applications, which require high quantity of computation especially in Blind Source Separation (BSS) problem.
- To overcome the computation cost of the hardware implementation of BSS, we found in the literature the neural network models that have been proposed in order to perform the parallel computation for separating the sources.
- However, the training time of the neural network models are in general very long.

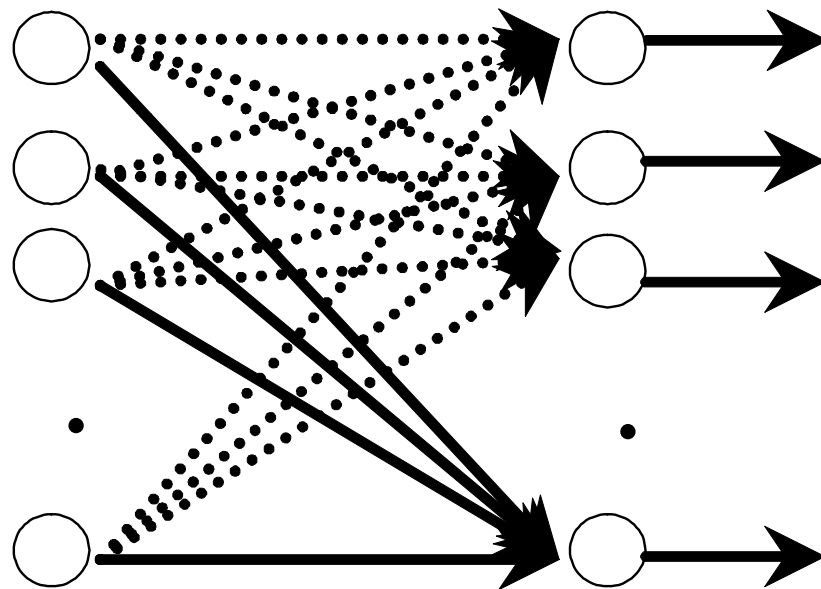


# PROBLEM SOLUTIONS

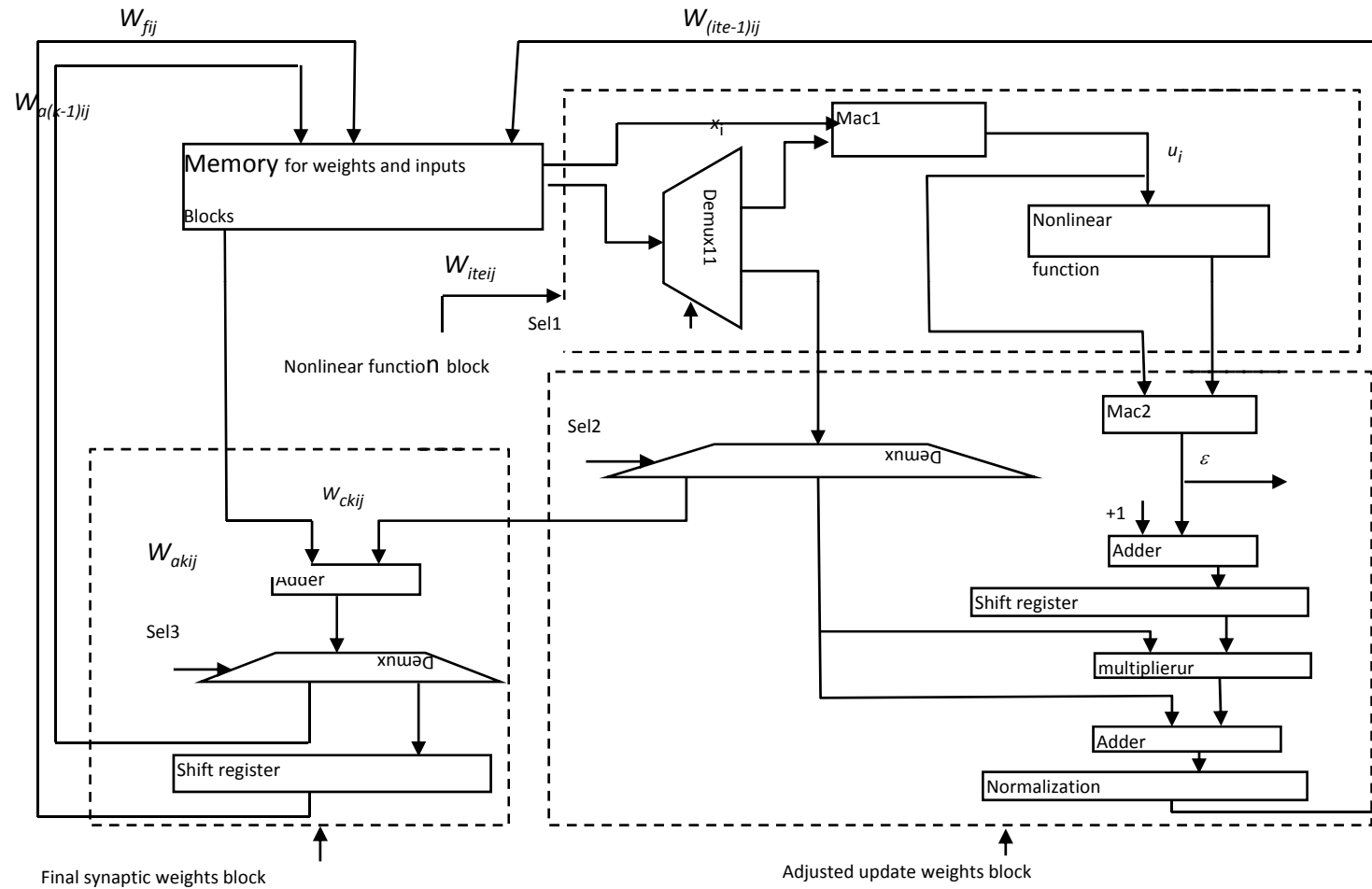
- To solve this problem, instead of using the software implementation for the training process of the network, the hardware implementation of the artificial neural network could be a reasonable solution that provides a parallel computation with a low cost of the computation time of the training phase of the network.
  - The designer of hardware implementation employs the technique of Field Programmable Gate Array (FPGA) because it has an advantage over the reprogrammable interconnection of their configurable logic blocks: flexible hardware architecture in terms of reducing the development time as well as the cost of manufacturing and so obtaining a rapid prototype.
  - Therefore, we can implement, with the advanced FPGA technology, the complex algorithms of neural network model for BSS with a low realization cost.
  - However, to avoid the problem of the limited resources in FPGA, we try to look for an optimal methodology of FPGA implementation of the ICA – based approach for BSS neural network model.
  - We used the Very High – speed Integrated Circuit Hardware Description Language (VHDL) as the programming tool for optimizing the hardware design of BSS neural network model.
  - The final configuration of the FPGA – based design for ICA – based approach for BSS neural network model will be detailed in the full version of the proposed paper.



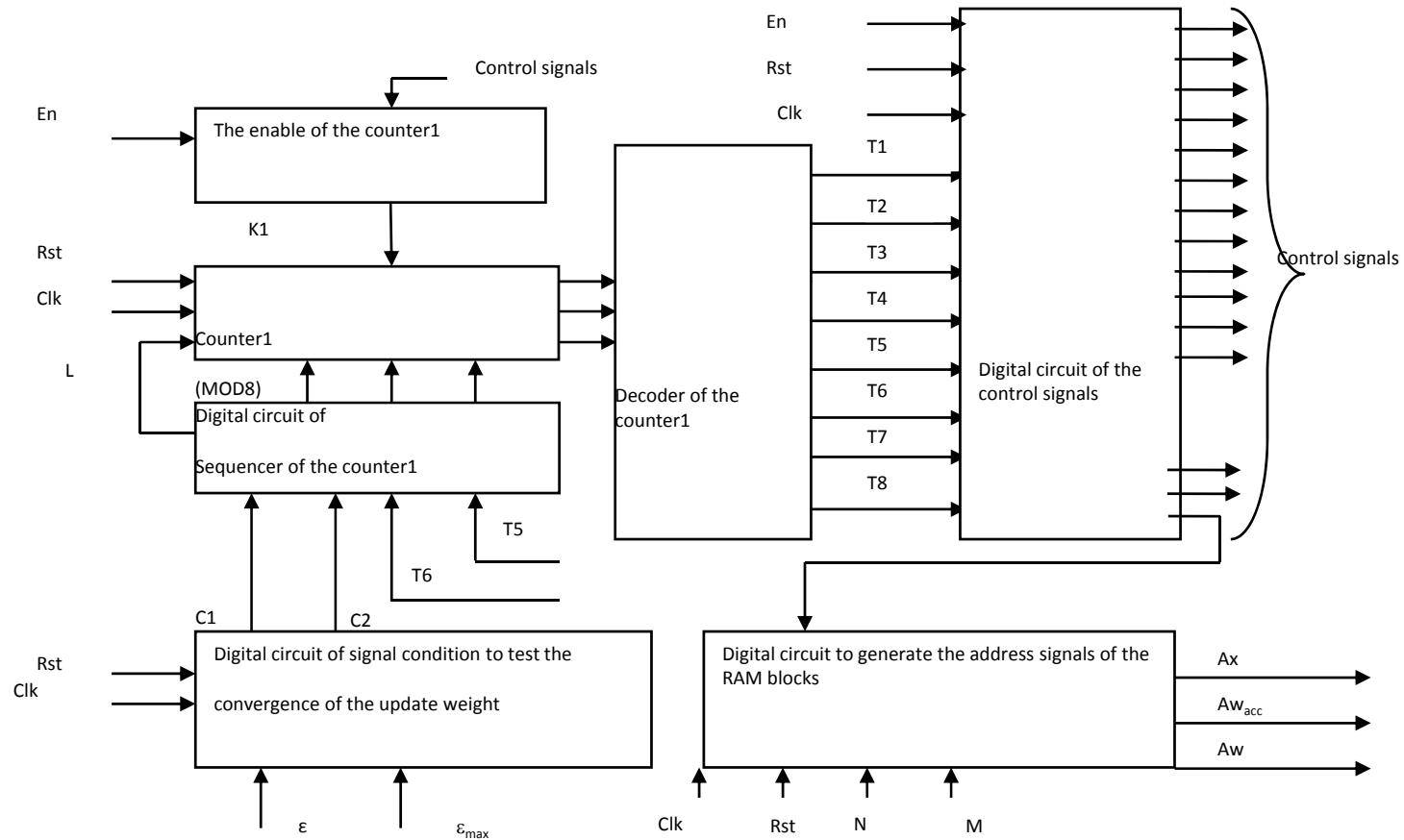
# THE NEURAL NETWORK MODEL OF ICA.



# DIGITAL CIRCUIT OF THE NEURON IMPLEMENTATION



# DIGITAL CIRCUIT OF THE CONTROL BLOCK IMPLEMENTATION



RESULTS FOR THE COMPARISON OF THE PROPOSED IMPLEMENTATION  
DESIGN OF NEURAL NETWORK MODEL OF ICA WITH OTHER FPGA  
IMPLEMENTATION DESIGNS PROPOSED IN THE LITERATURE FOR ICA  
ALGORITHM

Implementation	FPGA circuit	Cost (slices)	Learning time ( $\mu$ s)	Sample rates (kHz)	Frequency Max (MHz)
Implementation of ICNN[6]	Xilinx Virtex XCV 812 E	12271	6.44	–	50
Implementation of pICA algorithm[7]	Xilinx Virtex V 1000 E	11318	–	–	20.161
Implementation of BSS algorithm[8]	Xilinx Virtex-E family	–	–	8	64.4
Implementation of FastICA algorithm[9]	Altera company	–	5.2	192	50
Implementation of our algorithm	Xilinx Virtex II XC2V 8000	1500	17.351	57.53	185.580

